Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–III (NEW) EXAMINATION – WINTER 2023

Subject Code:3130704 Date:25-01-2024

Subject Name:Digital Fundamentals

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	List out various logic families. Also list characteristics of digital IC.	**03**
	(b)	State and prove De-Morgan's theorems using truth-tables.	**04**
	(c)	Implement AND, OR, EX-OR gates using NAND & NOR gates.	**07**
Q.2	**(a)**	Reduce the expression F = x'y'z +yz+ xz	**03**
	(b)	Convert the decimal Number 330.5 to base 4 and base 8.	**04**
	(c)	Design a Combinational circuit that convert Binary to BCD code converter.	**07**
		OR	
	(c)	Design a Combinational circuit that convert BCD to Excess 3 code converter.	**07**
Q.3	**(a)**	Minimize following Boolean function using K-map: Y(A,B,C,D) = Σ m(0, 1, 3, 5,6, 7, 10, 13,14, 15)	**03**
	(b)	Explain 4 – bit parallel adder with diagram.	**04**
	(c)	Design 2 - Bit Magnitude Comparator.	**07**
		OR	
Q.3	**(a)**	Design D FF using SR FF. Write truth table of D FF.	**03**
	(b)	Minimize following Boolean function using K-map: F(A,B,C,D) = Σ m(1, 5, 6, 12, 13, 14) + d(2, 4)	**04**
	(c)	Design 3-bit even parity generator circuit.	**07**
Q.4	**(a)**	Compare static RAM and dynamic RAM.	**03**
	(b)	Explain JK flip flop with its characteristic table and excitation table.	**04**
	(c)	Write a brief note on race around condition and its solution. Draw & explain the logic diagram of master-slave JK flip-flop.	**07**
		OR	
Q.4	**(a)**	Explain the types of ROM.	**03**
	(b)	Explain Look-ahead Carry generator	**04**
	(c)	Design a Synchronous counter with the following binary sequence: 0, 1, 3, 4,5, 7 and repeat. Use T – flip-flops	**07**
Q.5	**(a)**	Explain the working of a Counter.	**03**
	(b)	Explain R-2R ladder type D/A converter	**04**
	(c)	A combinational circuit is defined by the function F1 (A, B, C,) = Σ m (0,1,3,4) F2 (A, B, C,) = Σ m (1.2.3,4,5) Implement the circuit with a PLA having 3 inputs, 3 product term & 2 outputs.	**07**

OR

Q.5	**(a)**	Explain the working of SISO shift register.	**03**
	(b)	Explain the specification of D/A converter	**04**
	(c)	Describe operation of D/A converter with binary-weighted resisters	**07**

****