Enrolment No./Seat No_____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–VI (NEW) EXAMINATION – SUMMER 2024

Subject Code:3160712 Date:17-05-2024

Subject Name:Microprocessor and Interfacing

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Define (1) Microprocessor (2) System Bus (3) Instruction Cycle	**03**
	(b)	Explain 8085 Programming Model with diagram	**04**
	(c)	Draw and explain Pin diagram of 8085 Microprocessor	**07**
Q.2	**(a)**	Define (1) Accumulator (2) Program Counter (3) Stack Pointer	**03**
	(b)	Draw timing diagram of instruction MVI A, 32H	**04**
	(c)	Elaborate different addressing modes in 8085 with suitable examples	**07**
		OR	
	(c)	Draw the memory interface 4kB of EPROM with starting address from 0000H and 2kB of RAM with starting address followed by EPROM with 8085 Microprocessor	**07**
Q.3	**(a)**	Explain instruction format of 8085 instructions	**03**
	(b)	Describe any four arithmetic instructions in 8085 with examples	**04**
	(c)	Explain counters and time delay with suitable example. Also specify various applications of counters and time delay.	**07**
		OR	
Q.3	**(a)**	Explain classification of instructions based on byte size with examples	**03**
	(b)	Describe any four data transfer instructions in 8085 with examples	**04**
	(c)	Write an assembly language program in 8085 to arrange five 8-bit numbers in ascending order stored at memory location starting from 3000H	**07**
Q.4	**(a)**	Define Stack. Explain PUSH and POP instructions	**03**
	(b)	Explain classification of Interrupts in 8085 Microprocessor	**04**
	(c)	Draw and explain block diagram of 8255A	**07**
		OR	
Q.4	**(a)**	Differentiate IO-mapped IO and Memory-mapped IO	**03**
	(b)	Explain BSR Mode in 8255A	**04**
	(c)	Draw and explain block diagram of 8259A	**07**
Q.5	**(a)**	Describe flag register in 8086 Microprocessor	**03**
	(b)	Explain register organization of 80286 Microprocessor	**04**
	(c)	Draw and explain logical block diagram of 8086 Microprocessor	**07**
		OR	
Q.5	**(a)**	Describe protected virtual address mode in 80286 Microprocessor	**03**
	(b)	Explain concepts of segmentation in 8086 Microprocessor	**04**
	(c)	Draw and explain architecture of 80386 Microprocessor	**07**

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