

GUJARAT TECHNOLOGICAL UNIVERSITY**BE - SEMESTER-III(NEW) EXAMINATION – SUMMER 2023****Subject Code:3130704****Date:01-08-2023****Subject Name:Digital Fundamentals****Time:02:30 PM TO 05:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

	MARKS
Q.1 (a) Define the logic family properties: (i) fan in (ii) propagation delay (iii) power dissipation	03
(b) Convert the following number to the given base: (i) $(62)_{10} = (?)_2 = (?)_8$ (ii) $(AFB)_{16} = (?)_2 = (?)_8$	04
(c) Why NAND and NOR gates are called universal gates? Explain with appropriate example.	07
Q.2 (a) Explain the half subtractor with logic circuit.	03
(b) Minimized the boolean expression using K-map $f(A, B, C, D) = \sum m(0, 1, 5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$	04
(c) Design BCD to excess-3 converter.	07
OR	
(c) Design a circuit which compare two binary number whether $A > B$, $A = B$ or $A < B$.	07
Q.3 (a) Draw the circuit of a J-K flip-flop.	03
(b) Describe the operation of a shift register with suitable diagram.	04
(c) Design the four bit Johnson counter and explain the operation.	07
OR	
Q.3 (a) Explain different methods of Triggering of flip-flop.	03
(b) What are qualitative differences between parallel loading and serial loading in shift registers?	04
(c) Design a 3 bit synchronous counter using JK flip flop.	07
Q.4 (a) How can we describe the resolution of a D/A converter?	03
(b) A 10-bit D/A converter provides an analog output which has a maximum value of 10.23 volts. Find the resolution of this D/A converter.	04
(c) Explain the working of R-2R ladder type D/A converter.	07
OR	
Q.4 (a) Explain the types of A/D converters.	03
(b) A 10-bit D/A converter has a step-size of 10 mV. Determine the full-scale output voltage and the percentage resolution.	04

- (c) Describe the successive approximation A/D conversion principle with the neat diagram, explain this type of A/D converter. **07**
- Q.5** (a) Draw and explain the structure of a RAM cell. **03**
 (b) Implement using PLA **04**
 $f_1 = \sum m(0, 3, 4, 7)$
 $f_2 = \sum m(3, 5, 6, 7)$
 (c) Discuss in brief semiconductor memory organization and its operation. **07**
- OR**
- Q.5** (a) Compare the SRAMs and DRAMs. **03**
 (b) Implement the following Boolean expressions using a PROM. **04**
 $f_1(x_2, x_1, x_0) = \sum m(0, 1, 2, 5, 7)$
 $f_2(x_2, x_1, x_0) = \sum m(1, 2, 4, 6)$
- (c) What is a programmable LOGIC Array (PLA)? Describe with a logic diagram the principle of operation of a PLA. What are its advantages? **07**
