Q.1\*

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		GUJARAT TECHNOLOGICA	L UNIVERSITY
		BE- SEMESTER-III (NEW) EXAMINAT	ΓΙΟΝ – WINTER 2024
Subje	ct (	Code: 3130704	Date: 10-12-2024
Subje	ct l	Name: Digital Fundamentals	
Time:	10	:30 AM TO 01:00 PM	Total Marks: 70
Instruct	tion	s:	
	1.	Attempt all questions.	
	2.	Make suitable assumptions wherever necessary.	
	3.	Figures to the right indicate full marks.	
	4.	Simple and non-programmable scientific calculator	rs are allowed.
			MARKS
<b>).1</b> *	(a)	(a) Perform the following mathematical operation complement method.	ons using 2's <b>03</b>

 $(i) (9)_{10} + (-5)_{10}$ (ii)  $(3)_{10} - (8)_{10}$ 

	(b)	State and prove De-Morgan's theorems using truth-tables.	04
	(c)	Explain the characteristics of Digital ICs.	07
Q.2	(a)	Design a Full Adder circuit using basic logic gates.	03
	(b)	Design a modulo-6 ripple counter using T-Flip-flops.	04
	(c)	Design a 4-bit Binary to Gray Code Converter using K-map.	07
	(c)	<b>OR</b> Draw a two input TTL NAND gate and explain its operation.	07

## **Q.3** Explain Race Around Condition in JK flip flop. 03 (a) Design a 1 - bit Magnitude Comparator. 04 **(b)** Explain Hamming codes for error correction with a suitable example. 07 **(c)** OR Q.3 Find expression for the following and implement using logic gates. 03 **(a)** $F(A,B,C,D) = \pi M(0,2,3,6,7,8,9,12,13)$ Implement D flip flop using JK flip flop. **(b)** 04 Design a 4-bit twisted Ring Counter using JK flip flops. **(c)** 07

## **Q.4 (a)** Differentiate Synchronous Counters and Asynchronous Counters. 03 Implement the following using 8:1 MUX. 04 **(b)** $F = f(A,B,C,D) = \Sigma m(2,4,5,7,10,14)$ Design a synchronous BCD counter using J-K flip-flops. 07 (c) OR **Q.4** Implement full subtractor using 3:8 decoder and write a truth table. 03 **(a) (h)** Explain the specifications of Digital to Analog Converters. 04

	(~)	Emplain the specifications of Digital to Finalog Converters.	01
	(c)	Explain Successive Approximation type A/D converter.	07
Q.5	(a)	Differentiate Static RAM and Dynamic RAM.	03
	<b>(b)</b>	Write a short note on FPGA.	04
	(c)	Explain the operation of Dual-slope A/D converter.	07
		OR	
Q.5	<b>(a)</b>	Explain basic structure of a CCD (Charge Coupled Device).	03
	<b>(b)</b>	Write a short note on Programmable Array Logic.	04

(c) Explain various types of Read Only Memory. \*\*\*\*\*\*\*\*\*\*\*\* 07