Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – WINTER 2023

Subject Code:3140707 Date:19-01-2024

Subject Name: Computer Organization & Architecture

Time: 10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Draw the block diagram of a hypothetical basic computer.	**03**
	(b)	Show different ways to represent fixed-point positive integers including zero.	**04**
	(c)	Explain using flowchart the working of Booth's multiplication algorithm of signed-2's complement numbers.	**07**
Q.2	**(a)**	Which address sequencing capabilities are required in a control memory?	**03**
	(b)	Explain any four Arithmetic operations carried out by ALU.	**04**
	(c)	Discuss various memory hierarchies.	**07**
		OR	
	(c)	Explain the concept of Address Translation and working of the Translation Look-Aside Buffer.	**07**
Q.3	**(a)**	Discuss the importance of "control word" in a processor.	**03**
	(b)	Justify the use of STA instruction in assembly program with an example.	**04**
	(c)	Apply J K flip-flops to design a 3-bit synchronous binary counter.	**07**
		OR	
Q.3	**(a)**	Analyze the 20-bits microinstruction code format with 7 bit used for address.	**03**
	(b)	Apply BUN instruction in assembly program that needs to use a looped sub-routine to check a flag.	**04**
	(c)	Apply the combinational circuits to design a 4-bit adder/subtracter circuit which performs subtraction using 2's complement.	**07**
Q.4	**(a)**	Calculate and show the number of clock cycles required to execute BSA instruction.	**03**
	(b)	Write assembly program for the arithmetic shift-left operation on a number stored in register B. Stop the program in case of overflow.	**04**
	(c)	What is the fundamental difference between a subroutine call and an interrupt request? Analyze the possibility of common memory stack for both.	**07**
		OR	
Q.4	**(a)**	Show the working of LDA instruction using RTL.	**03**
	(b)	Write a program in assembly language to multiply two numbers in registers B and C in case the processor has only ADD instruction.	**04**
	(c)	A subroutine return address can be stored in an index register instead of a stack. Analyze the advantages and disadvantages of both configurations.	**07**
Q.5	**(a)**	A RAM operates with 8-bit data bus, 2 chip select lines and 7-bit address lines. Calculate the number of such RAM chips required to have 512 bytes of main memory.	**03**

	(b)	An address space is specified by 24 bits and the corresponding memory space by 16 bits. How many words are there in the address space and in the memory space?	**04**
	(c)	Discuss various Dynamic Arbitration Algorithms for Interprocessor Arbitration.	**07**

OR

Q.5	**(a)**	Calculate the size of a ROM chip which operates using 8-bit data bus, two chip select lines and 9-bit address bus.	**03**
	(b)	How many 128 x 8 RAM chips are needed to provide a memory capacity of 4096 bytes?	**04**
	(c)	Discuss in brief the interconnection structures of a multiprocessor system.	**07**

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