Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV(NEW) EXAMINATION – WINTER 2022

Subject Code:3140707 Date:15-12-2022

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			MARKS
Q.1	**(a)**	Draw the block diagram of 4-bit combinational circuit shifter.	**03**
	(b)	Construct diagram of common bus system of four 4-bits registers with diagram.	**04**
	(c)	What is the role of sequence counter(SC) in control unit? Interpret its concept with the help of its three inputs using diagram.	**07**
Q.2	**(a)**	List out names of eight main registers of basic computer with their symbolic name and purpose.	**03**
	(b)	Summarize following addressing modes with example. 1) Implied mode 2) Register mode	**04**
	(c)	Which are the different phases of Instruction Cycle? Describe Register transfer for fetch phase with its diagram.	**07**
		OR	
	(c)	Define: microinstruction; Identify different types of 16 bits instruction formats for basic computer using figure.	**07**
Q.3	**(a)**	Use BSA and BUN instruction with example and diagram.	**03**
	(b)	Criticize Three-Address Instructions and Zero address instruction with common example.	**04**
	(c)	Describe how control unit determine instruction type after the decoding using flowchart for instruction cycle.	**07**
		OR	
Q.3	**(a)**	Prepare flowchart of CPU-IOP communication.	**03**
	(b)	Differentiate RISC and CISC architecture.	**04**
	(c)	What is cache memory? Interpret direct addressing mapping with diagram.	**07**
Q.4	**(a)**	Draw and criticize memory hierarchy in a computer system.	**03**
	(b)	Write an Assembly level program for addition of 50 numbers.	**04**
	(c)	Draw the flowchart of first pass of the assembler and explain working of the same.	**07**
		OR	
Q.4	**(a)**	Interpret the following instructions: INP, ISZ and LDA	**03**
	(b)	Write an Assembly level program to move one block of data to another location.	**04**
	(c)	List out modes of transfer. Formulate direct memory access technique in detail.	**07**
Q.5	**(a)**	Summarize major hazards in pipelined execution.	**03**

	(b)	What is a data dependency conflict in instruction pipeline? Recommend solutions for data dependency conflicts.	**04**
	(c)	Demonstrate four-segment instruction pipeline in detail	**07**
		OR	
Q.5	**(a)**	Sketch Microinstruction code format. Quote BR and CD field in brief.	**03**
	(b)	Compare following terms: 1. Write through-cache and Write back cache. 2. Spatial locality and Temporal locality	**04**
	(c)	Elaborate flynn's classification scheme with proper diagram.	**07**

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