Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER–IV (NEW) EXAMINATION – WINTER 2021

Subject Code:3140707 Date:03/01/2022

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Explain three state buffers.	**03**
	(b)	Describe BUN and BSA memory reference instructions in detail.	**04**
	(c)	What is interrupt? Describe interrupt cycle with neat diagram.	**07**
Q.2	**(a)**	Differentiate assembly language and machine language.	**03**
	(b)	What is the need of common bus? Draw common bus cycle.	**04**
	(c)	Write an assembly language program to find whether the given number is prime or not.	**07**
		OR	
	(c)	Write an assembly language program to find factorial of the given number.	
Q.3	**(a)**	Define followings: 1. Control Memory 2. Control Word 3. Control Address Register	**03**
	(b)	Draw the flowchart of first pass of the assembler and explain working of the same.	**04**
	(c)	What is the significance of pipelining in computer architecture? Write a note on instruction pipeline.	**07**
		OR	
Q.3	**(a)**	What is address sequencing? Explain.	**03**
	(b)	Construct a 4-bit adder-subtractor circuit.	**04**
	(c)	What addressing mode means? Explain any three addressing modes in detail with example.	**07**
Q.4	**(a)**	Enlist the characteristics of RISC.	**03**
	(b)	Write a program to evaluate X = (a*b)/c+d in two address and three address instruction formats.	**04**
	(c)	Draw neat and clean flowchart for divide operation. Explain with example.	**07**
		OR	
Q.4	**(a)**	Differentiate isolated I/O and memory mapped I/O.	**03**
	(b)	Describe pipeline conflicts.	**04**
	(c)	What is cache memory address mapping? Compare and contrast direct address mapping and set-associative address mapping.	**07**
Q.5	**(a)**	What is the importance of virtual memory?	**03**
	(b)	Explain multiport memory and crossbar switch with reference to interconnection structures in multiprocessors.	**04**

	(c)	Assume a computer system uses 5 bit (1 sign + 4 Magnitude) registers and 2's complement representation. Perform multiplication of number 10 with the smallest number in this system using booth algorithm. Show step-by-step multiplication process.	**07**

OR

Q.5	**(a)**	What is cache coherence? Describe.	**03**
	(b)	A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. How many bits for the will be required for TAG field?	**04**
	(c)	Which are the different ways to transfer data to and from peripheral devices? Explain any one of them in detail.	**07**