Seat No.:	Enrolment No.

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER- I & II (NEW) EXAMINATION - WINTER 2019

Subject Code: 3110016 Date: 06/01/2020

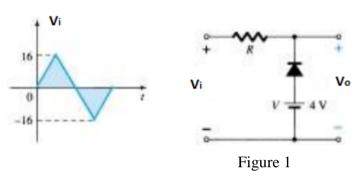
Subject Name: Basic Electronics

Time: 10:30 AM TO 01:00 PM Total Marks: 70

Instructions:

- 1. Attempt all questions.
- 2. Make suitable assumptions wherever necessary.
- 3. Figures to the right indicate full marks.

			Marks
Q.1	(a)	Draw the circuit diagram of Half wave rectifier.	03
	(b)	Explain the bridge rectifier with diagrams.	04
	(c)	Determine the Vo for the network shown in figure 1	07



- Q.2 (a) Explain Varactor diode and varistor. 03
 - (b) Why Zener diode can be used as voltage regulator? 04 Explain Zener as voltage regulator with necessary diagram
 - (c) Compare the logic families and explain any one of them. 07

OR

- (c) Explain Ex-OR and Ex- NOR gate with truth table and construct OR gate using diodes.
- Q.3 (a) Explain about DC load line and Bias point of transistor 03
 - (b) Explain the working of PIN Diode.
 (c) Briefly explain the h-parameters and draw h-parameter
 07
 - (c) Briefly explain the h-parameters and draw h-parameter based equivalent circuit for CE transistor and derive equation for input impedance, output impedance and voltage gain.

OR

- Q.3 (a) Write truth table of AND, NAND and NOR gates.(b) Explain the selection of a Q point for a transistor bias04
 - **(b)** Explain the selection of a Q point for a transistor bias circuit and discuss the limitations on the output voltage swing.
 - (c) Explain the difference between clipping and clamping circuit. A positive voltage clamping circuit and a positive voltage clipping circuit each have ±12 V square Wave input. Sketch the output waveform for each circuit.
- Q.4 (a) Draw voltage multiplier circuit. 03
 - (b) Explain Transconductance and switching in FET. 04

N.T. .1 .

(c)	Explain the Depletion region and drain characteristics of	
	n channel JFET.	
	OR	
(a)	Discuss about VI characteristic of Ideal Diode.	03
(b)	Explain FET as an Amplifier.	04
(c)	Determine the voltage Vo for the network of Figure 2.	07
	Give explanation for your answer.	
((a) (b)	n channel JFET. OR (a) Discuss about VI characteristic of Ideal Diode. (b) Explain FET as an Amplifier. (c) Determine the voltage Vo for the network of Figure 2.

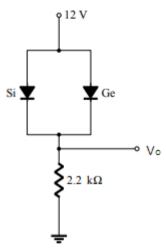


Figure 2

Q.5	(a)	a) Explain the working of Transistor as Switch			
	(b)	Write a short note on E MOSFET as an Amplifier.	04		
	(c)	Design a series noise clipping circuit which rectify the	07		
		noise signal with amplitude lower than $\pm V_F$.			
	OR				
Q.5	(a)	Explain the AC load line of transistor.	03		
	(b)	Draw and explain seven segment display.	04		
	(c)	Compare BJT with FET and explain D MOSFET.	07		
