Enrolment No./ Seat No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY

MASTER OF ENGINEERING - SEMESTER – III (OLD) EXAMINATION - SUMMER 2026

Subject Code: 3732605 **Date: 02/05/2026**

Subject Name: VLSI Test Principles and Architecture

Time: 10:30 AM TO 01:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Describe following terms in detail: a. Yield b. Fault Collapsing c. MTBF d. Bridging Fault	**07**
	(b)	Write short-note on random access scan design.	**07**
Q.2	**(a)**	How you will enhance the fault coverage? Explain three approaches for that.	**07**
	(b)	Explain SCOAP based combinational Controllability analysis technique.	**07**
		OR	
	(b)	What do you understand by stuck-at-faults? Draw 2-to-1 multiplexer circuit and discuss all possible stuck-at-faults for this circuit as well as find a set of optimum test vectors to detect these stuck-at-faults.	**07**
Q.3	**(a)**	Explain logic simulation flow for design verification.	**07**
	(b)	Explain PODEM algorithm for ATPG in detail.	**07**
		OR	
Q.3	**(a)**	Explain: D frontier and J-frontier with the help of example.	**07**
	(b)	Explain BIST Architectures for Circuits with Scan Chains.	**07**
Q.4	**(a)**	What do you understand by fault model? Differentiate single- and multiple fault models. Discuss transistor fault model taking 2-input NAND CMOS gate as an example.	**07**
	(b)	What is hazard? How it can affect circuit operation? Describe different types of hazards which can be observed during operation.	**07**
		OR	
Q.4	**(a)**	Describe following terms in detail: a. Critical Path Tracking b. Fault Sampling	**07**
	(b)	Explain different levels of abstraction in VLSI Testing.	**07**
Q.5	**(a)**	What is event driven simulation? Explain zero-event driven simulation with the help of example. Draw necessary flow chart for the same.	**07**
	(b)	Discuss various timing delay models. Clearly specify the difference between transport and inertial timing delay models by taking suitable example.	**07**
		OR	
Q.5	**(a)**	Explain the input scanning algorithm.	**07**
	(b)	Draw Clocked Scan cell design and explain its test operations with the help of waveforms.	**07**

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