Seat No./Enrollment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
MASTER OF ENGINEERING – SEMESTER 1 – EXAMINATION – SUMMER 2026

Subject Code: 3716301 **Date: 09/06/2026**

Subject Name: MOSFET Modeling for VLSI Circuits

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**

Q.1	**(a)**	Discuss the following types of MOSFET models for computational and memory efficiency : (i)Analytical model (ii)Table lookup model (iii)Empirical model	**07**
	(b)	Explain briefly diode current-voltage characteristics	**07**
Q.2	**(a)**	Draw a 4 terminal MOS transistor semiconductor structure and explain the structure in brief.	**07**
	(b)	Draw the cross section of a typical MOS capacitor and energy band diagrams of the components of MOS capacitor with no applied voltage.	**07**
		OR	
Q.2	**(b)**	Discuss the hot carrier effects in MOSFET.	**07**
Q.3	**(a)**	Draw the energy band diagrams of : (i)MOS capacitor with n+ degenerately doped polysilicon and p-type Si with no applied voltage (ii)MOS capacitor with n+ degenerately doped polysilicon and p-type Si with flat band condition	**07**
	(b)	What is the effect of the following on the gain of MOSFET (i) Cox (ii) Mu (iii) W	**07**
		OR	
Q.3	**(a)**	Define the following: (i) Work function of Metal (ii) Electron affinity of semiconductor (iii)Work function of p-type semiconductor (iv)Work function of n-type semiconductor (v)Flat band voltage	**07**
	(b)	Explain the deep implant model of non uniformly doped enhancement type MOSFET and its threshold voltage.	**07**
Q.4	**(a)**	Explain non uniformly doped depletion type MOSFET and its threshold voltage.	**07**
	(b)	Discuss the narrow width effect on threshold voltage of MOSFET.	**07**
		OR	
Q.4	**(a)**	Draw the equivalent circuit of a MOS capacitor. Explain the effect of applied gate voltage on gate capacitance.	**07**
	(b)	Discuss the Shichman-Hodges MOSFET DC model for SPICE level 1 along with its key parameters.	**07**

Q.5	**(a)**	Discuss MOSFET capacitance model for SPICE level 2 along with its key parameters	**07**
	(b)	Explain briefly the Berkeley SPICE MOSFET models with their key features.	**07**

OR

Q.5	**(a)**	Discuss the components of MOSFET capacitances (i)Intrinsic part (ii) Extrinsic part	**07**
	(b)	Discuss the key features of BSIM - IMG model for multigate FET architectures.	**07**

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