Seat No./Enrollment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
BACHELOR OF ENGINEERING – SEMESTER 5 – EXAMINATION – SUMMER 2026

Subject Code: 3154704 **Date: 02/06/2026**

Subject Name: VLSI TECHNOLOGY AND DESIGN

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Discuss methods to estimate interconnect parasitic.	**03**
	(b)	Why we need to scale VLSI Design? Compare constant field and constant voltage scaling.	**04**
	(c)	Describe MOS System under External Bias with neat sketch of cross sectional view and energy band diagram. Also derive depletion region depth equation.	**07**
Q.2	**(a)**	List packaging technology used for VLSI chips.	**03**
	(b)	Describe Regularity, Modularity and Locality in VLSI Design.	**04**
	(c)	Draw and explain 'Y' chart for the VLSI design flow.	**07**
		OR	
Q.2	**(c)**	Derive the equation for propagation delay during high-to-low transition of output of CMOS inverter circuit with C_{load} as load capacitance.	**07**
Q.3	**(a)**	Compare Semi-custom and Full custom VLSI design style.	**03**
	(b)	Implement following Boolean expression using CMOS inverter. $Z= (A(D+E)+BC)'$	**04**
	(c)	Derive the equation for drain current (I_D) of MOSFET using Gradual Channel Approximation.	**07**
		OR	
Q.3	**(a)**	Why in symmetrical and ideal CMOS inverter required $(W/L)_p \approx 2.5(W/L)_n$. Justify.	**03**
	(b)	Derive Critical voltages V_{IL} and V_{IH} of CMOS inverter.	**04**
	(c)	Explain Fabrication steps of n-MOSFET with neat sketch.	**07**
Q.4	**(a)**	Explain MOSFET capacitance in brief.	**03**
	(b)	Realize $F=AB' + A'B$ function using Transmission Gates.	**04**
	(c)	Derive equation for Threshold Voltage and also describe substrate bias effect.	**07**
		OR	
Q.4	**(a)**	Draw resistive load inverter circuit and its VTC curve.	**03**
	(b)	Design NOR gate based CMOS SR latch circuit.	**04**
	(c)	Explain CMOS Transmission gate.	**07**
Q.5	**(a)**	Explain noise margin.	**03**

	(b)	What is photo lithography? Differentiate positive and negative photo resist material.	**04**
	(c)	Derive equation of Switching Power Dissipation for CMOS inverter with ideal step input.	**07**

OR

Q.5	**(a)**	What is hot carrier effect and punch through in small geometries devices?	**03**
	(b)	Draw the CMOS implementation of D-latch.	**04**
	(c)	Write a program to implement 4x1 multiplexer using 2x1 multiplexers in Verilog HDL.	**07**

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