Seat No./Enrollment No.: _____

GUJARAT TECHNOLOGICAL UNIVERSITY
BACHELOR OF ENGINEERING – SEMESTER 5 – EXAMINATION – SUMMER 2026

Subject Code: 3154107 **Date: 21/05/2026**

Subject Name: Computer Architecture

Time: 02:30 PM TO 05:00 PM **Total Marks: 70**

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

Q.1	**(a)**	Explain the basic structure of a computer system.	**03**
	(b)	Explain the concept of addressing modes in MIPS. Illustrate with an example how base addressing works in load/store instructions.	**04**
	(c)	State various phases of instruction cycle.	**07**
Q.2	**(a)**	Divide $1{,}001{,}010_{ten}$ by 1000_{ten}.	**03**
	(b)	Write down steps for binary floating point addition.	**04**
	(c)	Assume A = + 7 and B = + 3, apply Booth algorithm for multiplying A and B. Make necessary assumptions if required.	**07**
		OR	
Q.2	**(c)**	State and Explain any seven logic micro operation with example.	**07**
Q.3	**(a)**	Explain pipeline conflicts in brief.	**03**
	(b)	Explain arithmetic pipeline.	**04**
	(c)	Describe how control unit determine instruction type after the decoding using flowchart for instruction cycle. Describe importance of SC(Sequence Counter).	**07**
		OR	
Q.3	**(a)**	List out names of registers of basic computer with their symbolic name and purpose.	**03**
	(b)	What is a data dependency conflict in instruction pipeline? Recommend solutions for data dependency conflicts.	**04**
	(c)	Explain pipelining technique. Draw the general structure of four segment pipeline.	**07**
Q.4	**(a)**	Write a short note on Graphical Processing Unit.	**03**
	(b)	Write a note on crossbar switch interconnection structure with block diagram.	**04**
	(c)	Elaborate flynn's classification scheme with proper diagram.	**07**
		OR	
Q.4	**(a)**	Differentiate tightly coupled and loosely coupled multiprocessor systems.	**03**
	(b)	Write a short note on SIMD array processor.	**04**
	(c)	Discuss in brief the interconnection structures of a multiprocessor system.	**07**
Q.5	**(a)**	Illustrate and analyze the memory hierarchy in a computer system with strengths and weaknesses of each level.	**03**

(b) Write a short note on content addressable memory. **04**

(c) Write a short note on virtual memory. **07**

OR

Q.5 **(a)** Explain the role of associative memory. **03**

(b) Explain in brief daisy chain priority interrupt. **04**

(c) What is cache memory? Interpret direct addressing mapping with diagram. **07**

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