

GUJARAT TECHNOLOGICAL UNIVERSITY**BE- SEMESTER– IV EXAMINATION – SUMMER 2026****Subject Code:3142408****Date:28-05-2026****Subject Name:Analog & Digital Circuits****Time:10:30 AM TO 01:00 PM****Total Marks:70****Instructions:**

1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.
4. Simple and non-programmable scientific calculators are allowed.

MARKS

- | | | | |
|------------|-----|--|-----------|
| Q.1 | (a) | Define the following | 03 |
| | a) | Input Offset Current | |
| | b) | Slew Rate | |
| | c) | Input Bias Current | |
| | (b) | Compare inverting and non-inverting op-amps. | 04 |
| | (c) | Draw the block schematic of a typical operational amplifier Op-Amp and briefly explain the function of each block. | 07 |
| Q.2 | (a) | Draw and explain working of zero crossing detector | 03 |
| | (b) | Explain voltage follower with it's application. | 04 |
| | (c) | With neat circuit diagram explain the working of an Integrator with relevant waveforms. | 07 |
| OR | | | |
| | (c) | Draw the circuit op-amp as differentiator and explain with necessary waveforms. | 07 |
| Q.3 | (a) | Compare SOP and POS | 03 |
| | (b) | Compare combinational logic circuit with sequential logic circuit | 04 |
| | (c) | Minimize following Boolean function using K-map:
$F(A,B,C,D) = \Pi M(1, 2, 3, 8, 9, 11, 14) \cdot d(7, 15)$ | 07 |
| OR | | | |
| Q.3 | (a) | Compare Multiplexer and Demultiplexer. | 03 |
| | (b) | Explain Full adder logic circuit. | 04 |
| | (c) | Minimize following Boolean function using K-map:
$Y(A,B,C,D) = \Sigma m(0, 3, 5, 6, 9, 10, 12, 15)$ | 07 |
| Q.4 | (a) | Explain Master-Slave J-K flip-flop configuration | 03 |
| | (b) | Write a short notes on Parallel in serial out shift register | 04 |
| | (c) | Draw 4-bit down counter; explain its working with timing diagram and truth table. | 07 |
| OR | | | |
| Q.4 | (a) | Classify the various modes of operation of shift register. | 03 |
| | (b) | Draw & explain in detail the logic diagram & the truth table of clocked SR flip-flop | 04 |
| | (c) | Design 4-bit up/down ripple counter | 07 |
| Q.5 | (a) | Sketch sample and hold circuit and explain its working. | 03 |
| | (b) | Define following specification of ADC | 04 |
| | | 1)Conversion Time | |
| | | 2)Resolution | |
| | | 3)Quantization | |

	(c)	Draw & explain R-2R ladder D/A converter with necessary equations.	07
		OR	
Q.5	(a)	Compare various D/A converters	03
	(b)	Write a brief note on quantization and encoding.	04
	(c)	Explain working of Successive approximation type ADC	07
