Seat No./Enrollment No.: _____

# GUJARAT TECHNOLOGICAL UNIVERSITY
## BACHELOR OF ENGINEERING – SEMESTER 3 – EXAMINATION – SUMMER 2026

**Subject Code: 3130704** **Date: 02/07/2026**

**Subject Name: Digital Fundamentals**

**Time: 02:30 PM TO 05:00 PM** **Total Marks: 70**

**Instructions:**

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

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| **Q.1** | **(a)** | Convert the decimal number 163 to its equivalent binary, octal and hexadecimal forms. | **03** |
| | **(b)** | Convert the BCD number 10010111 into its equivalent decimal and Excess-3 code. | **04** |
| | **(c)** | What do you mean by universal gates, and which gates are universal? Convert NAND gate to OR gate. Convert NOR gate to AND gate. | **07** |
| **Q.2** | **(a)** | Define : priority encoder, SOP and POS | **03** |
| | **(b)** | Analyze the conditions for a 'Don't Care' term in K-map simplification and simplify the expression $F(W,X,Y,Z)=\sum m(1,3,7,11,15)$ with Don't Care $d(W,X,Y,Z)=\sum d(0,2,5)$. | **04** |
| | **(c)** | Design a full subtractor circuit using basic logic gates. Also write its truth table. | **07** |
| | | OR | |
| **Q.2** | **(c)** | Implement a 4×16 decoder using two 3×8 decoders. | **07** |
| **Q.3** | **(a)** | Distinguish between synchronous and asynchronous (ripple) counters based on their clocking mechanism. | **03** |
| | **(b)** | Define the term : 'state table' for a sequential circuit, ripple counter | **04** |
| | **(c)** | Draw a neat diagram of a 4-bit right shift register and explain its operation | **07** |
| | | OR | |
| **Q.3** | **(a)** | Analyze the state transition diagram for a Johnson (twisted ring) counter and explain its counting sequence for 4 flip-flops. | **03** |
| | **(b)** | Define the term 'ring counter' and briefly explain how it differs from a Johnson counter. | **04** |
| | **(c)** | Explain J-K flip-flop and T flip-flop along with diagram and excitation table. | **07** |
| **Q.4** | **(a)** | Compare the weighted resistor D/A converter with the R-2R ladder D/A converter based on complexity, accuracy and ease of expansion. | **03** |
| | **(b)** | Define the term 'Quantization' and 'Encoding' in the context of A/D conversion. | **04** |
| | **(c)** | Evaluate the advantages and disadvantages of the dual slope A/D converter compared to the Successive Approximation A/D converter | **07** |
| | | OR | |
| **Q.4** | **(a)** | Describe the operation of a Successive Approximation A/D (SAR) converter and state its main specification regarding conversion time. | **03** |
| | **(b)** | List the main components of an Analog-to-Digital conversion process | **04** |
| | **(c)** | Justify the use of an R-2R ladder network over a weighted resistor network for high-resolution D/A converters. Evaluate the advantages and disadvantages of the both. | **07** |
| **Q.5** | **(a)** | Define Read Only Memory (ROM) and list its different types. | **03** |

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|---|---|---|---|
| | **(b)** | Describe the architecture and use of Field Programmable Gate Arrays (FPGAs). | **04** |
| | **(c)** | Design a simple combinational logic function $F(A,B,C)=\sum m(0,1,2,5,7)$ and implement it using a Programmable Logic Array (PLA), clearly showing the internal connections. | **07** |

OR

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|---|---|---|---|
| **Q.5** | **(a)** | Differentiate between static RAM (SRAM) and dynamic RAM (DRAM). | **03** |
| | **(b)** | Describe the concept of memory organization in semiconductor memories | **04** |
| | **(c)** | Implement the logic function $F(X,Y,Z)=\sum m(1,2,4,7)$ using a ROM as a PLD, showing the memory organization. | **07** |

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