Seat No.: _____ Enrolment No._____

GUJARAT TECHNOLOGICAL UNIVERSITY

BE - SEMESTER– IV(NEW) EXAMINATION – SUMMER 2023

Subject Code:3140707 Date:13-07-2023

Subject Name:Computer Organization & Architecture

Time:10:30 AM TO 01:00 PM Total Marks:70

Instructions:

1. **Attempt all questions.**
2. **Make suitable assumptions wherever necessary.**
3. **Figures to the right indicate full marks.**
4. **Simple and non-programmable scientific calculators are allowed.**

			Marks
Q.1	**(a)**	Write the name of basic computer registers with their functionalities.	**03**
	(b)	Discuss 4-bit binary adder with neat diagram.	**04**
	(c)	Enlist various kinds of addressing modes. Explain any five of same and support your answer by taking small example.	**07**
Q.2	**(a)**	Write sequence of microoperations to execute the following instructions: - AND - STA	**03**
	(b)	Write assembly language program to subtract two numbers.	**04**
	(c)	Write two address, one address and zero address instructions program for the following arithmetic expression: X = (A + B) * (C – D / E) + F * G	**07**
		OR	
	(c)	Assume A = + 6 and B = + 7, apply Booth algorithm for multiplying A and B. Make necessary assumptions if required.	**07**
Q.3	**(a)**	Explain Flynn's classification for computers in brief.	**03**
	(b)	Draw the flowchart for first pass of assembler and explain the same in brief.	**04**
	(c)	Elaborate CPU-IOP communication.	**07**
		OR	
Q.3	**(a)**	Explain pipeline conflicts in brief.	**03**
	(b)	Discuss three state bus buffers with neat diagram.	**04**
	(c)	Write a detailed note on associative memory.	**07**
Q.4	**(a)**	Explain DMA in brief.	**03**
	(b)	Write a note on SIMD array processor.	**04**
	(c)	A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. 1. How many bits are there in operation code, the register code part and the address part? 2. Draw the instruction word format and indicate the number of bits in each part. 3. How many bits are there in the data and address inputs of the memory?	**07**
		OR	
Q.4	**(a)**	Write a brief note on memory hierarchy.	**03**
	(b)	In certain scientific computations it is necessary to perform the arithmetic	**04**

operation (A_i + B_i) * (C_i + D_i) with a stream of numbers. Specify pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 4.

(c) Discuss microprogrammed control organization with neat diagram. **07**

Q.5 **(a)** Perform A – B (subtract) operation for the following numbers using signed magnitude number format. (Write necessary assumptions if required) **03**

A = + 11 and B = - 6

(b) Explain status bit conditions with neat diagram. **04**

(c) Discuss cache coherence problem in detail. **07**

OR

Q.5 **(a)** Write the difference(s) between arithmetic shift left and logical shift left instruction. Support your answer with proper illustration. **03**

(b) State the differences between RISC and CISC. **04**

(c) Explain any two types of mapping procedures when considering the organization of cache memory. **07**

****