GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (EMBEDDED SYSTEM) (54)

EMBEDDED AND VLSI SIGNAL PROCESSING

SUBJECT CODE: 2725406

SEMESTER: II

Type of course: Signal Processing and VLSI Design

Prerequisite: Fundamental knowledge of digital signal processing and basic concept of VLSI

Rationale: Students of ME in Embedded Systems must possess a good understanding of concepts of signal processing and VLSI Domain. Students also must learn about HDL Programming. This is one of the foundation courses which are required for design and implementation using CPLD and FPGA for applications demanding low-power and high frequency.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2#	2	5	70	30	20	10	10	10	150

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Digital Signal Processing Overview:** Signals, Systems and Signal processing, classification of signals, Linear Time Invariant (LTI) System, Convolution, And Correlation: Properties and application of correlation, Sampling, FFT Algorithms and Fundamentals of FIR and IIR Filters.	**10**	**20**
2	Introduction to hardware description language (VHDL): Structural, Behavioral and Data Flow modeling, Concurrent and Sequential VHDL, VLSI Design methodologies, basic steps of fabrication process flow, FPGA Technology and its Applications, The FPGA technology roadmap, FPGA Architecture and its building blocks, Technology mapping for FPGAs.	**08**	**20**
3	Design and Implementation using CPLD and FPGA and need of Floor Planning and placement tools, Input/output blocks and Configurable Logic Blocks, FPGA Families and Sources, xiling 3000 series logic cell with its CLB.	**08**	**20**
4	Static Characteristics of MOS Inverter, Combinational MOS Logic Circuits, Shift Registers, RAM and ROM (memory), Multiplexers design.	**08**	**20**
5	DSP Arithmetic Essentials, Fundamental of adders and Sequential MOS Logic Circuits, FPGA design for digital filters: FIR and IIR Filter.	**08**	**20**
	Total	**42**	**100**

Reference Books:

1. John G. Proakis, "Digital Signal Processing" Principles, Algorithms and applications, Prentice-Hall of India, 2007, fourth edition.
2. K. K. Parhi, "VLSI Digital Signal Processing Systems- Design and Implementation", John Wiley & Sons, Inc., 1999, fourth edition.
3. S.M. Kang, "CMOS Digital Integrated Circuits", McCraw Hill, third edition

4. J. Bhasker, VHDL Synthesis Primer, Pearson Education Asia, Low Price, Edition, second edition
5. Uwe MeyerBaese: "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2001, second edition.
6. Xilinx and Altera Application notes on the architecture of FPGA and CPLD

Course Outcome:

Students will get sound knowledge in following topics which are required for advanced VLSI circuits design and Filter Design using HDL Coding

1. Analog to Digital Convert design
2. FPGA Design for digital Filter
3. VHDL coding for any digital circuits
4. Memory design (RAM and ROM)
5. Design and implementation using CPLD and FPGA
6. Static and dynamic characteristics of CMOS.

List of Experiments:

1	Introduction to various signal generation MATLAB/CCS.
2	Generation of various signals and their implementation on kit.
3	Convolution and correlation of the various signals.
4	(a) Various Transformation: DCT, DFT, DTFT, FFT, FT, STFT, ZT (b) Inverse Transformation: (DCT, DFT, DTFT, FFT, FT, STFT, ZT)
5	FIR filter design and their implementation
6	IIR filter design and their implementation
7	a) To Introduction to Hardware Description language (VHDL) and Familiar with Quartus-II Software (Programming Tool) b) Implementation of basic logic gates, universal logic gates and its testing.
8	Write a VHDL code for 4:1 Multiplexer and design and verify 8:1 Multiplexer with structural modeling.
9	(a) Write a program for 8:3 Decoders with case statement. (b) Write a program for 3:8 Decoders with various statements and its testing.
10	Design and verify JK Flip-flop and D Flip-flop with behavioral modelling.
11	Implementation of BCD Counter and up-down counter and its testing. Verify the functionality of shift registers.
12	Design and verify the functionality of Finite State Machines

Design based Problems (DP)/Open Ended Problem:

1. Digital Filters Design and their implementation on FPGA kit.
2. Design and Implementation of ADC with any layout design tool.
3. Design and Implementation of RAM.
4. CMOS design of various digital circuits

Major Equipments:

i. Personal Computer
ii. ALTERA DE-I and DE-II Board
iii. DSP (CCS) kit
iv. DSO

List of Software:

MATLAB, Quartus-II, LT-SPice (**Open Source Software)**

Learning website:

www.nptel.ac.in

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website