GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (EMBEDDED SYSTEM) (54)

DIGITAL SIGNAL PROCESSORS: ARCHITECTURE AND PROGRAMMING

SUBJECT CODE: 2725402

SEMESTER: II

Type of course: Digital Signal Processor Architecture

Prerequisite: Fundamental knowledge of Digital Signal Processing

Rationale: The students of M. E. Embedded Systems should be exposed with real-time signal processing. The syllabus of this subject will provide opportunity to implement various digital signal processing algorithms on fixed and floating-point digital signal processors.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	0	2#	4	70	30	20	10	10	10	150

Content:

Sr. No.	Course Content	Teaching Hours	Module Weightage
1	**Introduction to Digital Signal Processors** Programmable DSP Processors (P-DSPs), Multiplier and Multiplier Accumulator (MAC), modified bus structures and memory access schemes in P-DSPs, Multiple Access Memory, VLIW architecture, Pipelining, Special addressing modes in P-DSPs, On-chip peripherals	10	15%
2	**Implementation Considerations** Fixed-point & floating-point numbers and arithmetic, Quantization, Overflow and solutions, Rounding and truncation, Real-time Implementation Considerations: Signal converters, Stream processing, Block processing, Vector processing; Hardware Interfacing: External memory interfacing, Serial & parallel port interfacing, Host-port interfacing, Multiprocessing techniques	12	15%
3	**Fixed-point Digital Signal Processors: TMS320C54x** Introduction, Bus structure, Central Arithmetic Logic Unit (CALU), Auxiliary Register ALU (ARALU), Index register, Block Move Address register, Block Repeat registers, Assembler directives; Architecture overview, CPU, Addressing modes, Instruction set: Addition/Subtraction instructions, Load/Store instructions, Move instructions, Multiplication instructions, NORM and Program control instructions; pipelining in C54x processor	16	20%

4	**Floating- Point Digital Signal Processors: TMS320C67x** Introduction, Bus Structure, Central ALU, Auxiliary Register ALU, Index Register, Auxiliary Register ALU, Block Move Address Register, Block repeat registers, parallel logic unit, memory-mapped registers, program controller, flags in status register, on-chip memory, on-chip peripherals, Assembly Language Syntax, Addressing Modes and instructions, pipelining in C67x processor	24	35%
5	**Applications of Digital Signal Processors** FIR and IIR filtering applications, Adaptive filtering, FFT, Discrete Cosine Transform (DCT) and Other transforms; Real-time applications in Automation and Process control, Communication and telecom, Health tech, Consumer and Portable electronics	10	15%

Reference Books:

1. Digital Signal Processors: Architectures, Implementations and Applications by Sen M. Kuo and Woon-Seng S. Gan, Pearson Education
2. Digital Signal Processors: Architectures, Programming and Applications by B Venkatramani and M Bhaskar, TMH

Course Outcome:

Students will get sound knowledge in following topics which are required for real-time digital signal processing algorithms.

1. Digital signal processor architecture
2. Programmable DSPs (P-DSP)
3. Fixed point DSP architecture and programming
4. Floating point DSP architecture and programming
5. Real time implementation of digital signal processing algorithms

List of Experiments:

EXP. NO.	NAME OF THE EXPERIMENT
1.	Introduction to Code composer studio (CCS)
2.	i. Matrix/vector multiplication using TMS320Cxx ii. Sine generation with 4 points using TMS320Cxx
3.	i. Multiplication of two arrays using TMS320Cxx ii. Background for digital filtering using TMS320Cxx
4.	Data acquisition (Input) and Display (output) using TMS320Cxx
5.	FIR lowpass filter simulation with 11 coefficients using TMS320C3xx
6.	i. Eight-point complex FFT using C code ii. Eight-point FFT with real-valued Input, using mixed C and TMS320Cxx code
7.	Adaptive filter for noise cancellation using C code
8.	i. FIR filter design using MATLAB ii. IIR filter design using MATLAB
9.	Discrete cosine transform (DCT) implementation on TMS320Cxx
10.	Mini Project based on above algorithms

Design based Problems (DP)/Open Ended Problem:

1. Real time FIR/IIR filter incorporating pseudorandom noise as input, using TMS320C67x
2. Real-time adaptive filter for noise cancellation using TMS320C67x
3. Filtering a speech/audio signal to remove noise using TMS320C67x
4. Design a notch filter for removing powerline noise from ECG signal using TMS320C67x
5. Design a high pass filter for removing baseline wandere from ECG signal using TMS320C67x

Major Equipment:

i. TMS320C54x and TMS320C67x kits
ii. Personal Computer

List of Open Source Software/learning website:

Code Composer Studio, Matlab

www.nptel.ac.in

www.rice.edu

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website