GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (VLSI SYSTEM DESIGN) (42)
VLSI SIGNAL PROCESSING
SUBJECT CODE: 2724209
SEMESTER: II

Type of course: Major Elective_II

Prerequisite: HDL and High Level Synthesis

Rationale: To learn the theory and practice of VLSI in Signal Processing and Communications. To introduce the basic approaches and methodologies for VLSI design of signal processing and communication Systems. To provide hands-on VLSI system design experience using hardware description language (HDL).

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2#	2	5	70	30	20	10	10	10	150

Content:

Sr. No	Content	Total Hrs.	% Weightage
1	Introduction to Digital Signal Processing Systems : Introduction**,** DSP Applications, DSP Implementations & Its Limitations, Typical DSP Algorithms, Area, Speed Power Tradeoffs, Representation Methods of DSPs.	8	15
2	Iteration Bound: Introduction, DFG Representations, Loop Bound and Iteration Bound , Algorithms to compute Iteration Bounds, Iteration Bound of Multirate Data Flow Graphs	6	15
3	Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing, Pipeline & Parallel Processing for Low Power, Retiming & Its Properties, Retiming Techniques	6	15
4	Unfolding & Folding : Introduction, Algorithms, Properties and applications of Unfolding, Folding Transformation, Register Minimization Techniques, Folding of Multirate Systems,	8	15
5	Systolic Architecture Design, Systolic Array Design Methodology, FIR Systolic Arrays, Fast Convolution, Algorithms, Algorithmic Strength Reduction in filter and Transforms, Pipelined and Parallel Recursive and Adaptive Filters, Scaling and Round off Noise	8	15
6	Bit level Arithmetic Architectures, Redundant Arithmetic, Numerical Strength Reduction,	6	10
7	Low Power Design, Programmable Digital Signal Processors	6	15

Reference Books:

1. K.Parthi, "VLSI Digital Signal processing systems, Design and implementation", Wiley, Inter Science, 1999.
2. Uwe, Meyer-Bease, Digital Signal Processing with FPGA, Springer-India 2003
3. Mohammed Isamail and Terri Fiez, "Analog VLSI Signal and Information Processing", Mc Graw-Hill, 1994.
4. S.Y. Kung, H.J. White House, T.Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice-Hall, 1994.
6. S.Y.Kung, VLSI Array Processors, Prentice-Hall, 1988.
7. P.Lapsley, J. Bier, A. Shoham and E.A. Lee, Dsp Processor Fundamentals: Architectures and Feature, Wiley/IEEE, 2001.
8. P.Pirsch, Architecture for Digital Signal Processing, Wiley, 1998.
9. V.K.Madisetti, VLSI Digital Signal Processors, Butterworth-Heinemann/IEEE press, 1995.
10. M.Mehendale and S.D.Sherlekar, VLSI Synthesis of DSP Kernels, Kluwer, 2001.
11. Bateman and I.Paterson-Stephens, The DSP Handbook, PH/Pearson, 2002.
12. S.M. Kuo, Digital Signal Processors: Architectures, Implementation and Applications, PH/Pearson, 2004.
13. L.Wanhammar, DSP Integrated circuits, AP, 1997.
14. M.A. Richards, A.J. Gadient and G.A.Frank, Rapid Prototyping of Applications, PH/Pearson, 1997.
15. B.Venkataramani and M. Bhaskar, Digital Signal Processing: Architecture, Programming and Applications,TMH,2002
16. E.E.Swartzlander, Application Specific Processors, Kluwer, 1997.
17. U.Meyer-Baese, DSP with FPGAs, Springer- Verlag.

Course Outcome:

After learning the course the students should be able to:

1. Review digital signal processing, computer architecture and coding.
2. Design methodology of VLSI and building DSP blocks.
3. Transform of high speed - low power algorithms and mapping techniques.
4. Write application code DSP implementation platforms (programmable DSP's,).
5. Develop case studies.
6. To expose students to the advanced HDL design techniques and methodology and industrial standard EDA tools in electronic design. The content will also allow students to gain hands-on experience with the most recent digital design techniques.

List of Experiments:

Sr. No.	List of Experiments
1	Design the Following: a) Tristate Buffer b) Binary to Grey Converter c) Design 2X1, 4X1 and 8X1 multiplexers using gate level and data flow modeling. d) Ripple carry adder e) Carry look ahead adder f) Priority Encoder Circuit
2	Design the Following: a) Model a D-latch b) Positive edge triggered DFF with asynchronous reset.

	c) Positive edge triggered DFF with synchronous reset
3	Design a VHDL Code for Edge Detector
4	Design an sequence detector for Sequence 1110
5	Design an 8bit Shift Left and Shift Right Register
6	Design an 8 bit SIPO, PISO and SISO registers; whose values initialized to 00h upon reset and AAH upon the application of load signal for one clock.
7	Design a pulse stretching circuit that stretches the pulse of one clock duration to a pulse of 3 clock duration.
8	Design a 4 bit up down counter that should count up if Dir signal is high and should count down if the Dir signal is low. The initial value of the counter is loaded from a 4 bit bidirectional data bus upon the application of the load signal. The count can be read whenever monitor signal goes high.
9	Design an 8bit Bidirectional Data Bus which is used to read and write from an 8-bit register. The data on the register has to be driven onto the bus if the read signal is high and data on the bus has to be written into the register if the write signal is high. Otherwise the bus has to be tristated.
10	Design a FIFO
11	Configure a 1024x8 RAM and write AAh into the RAM whenever wr_en goes high and read the data stored in the RAM whenever rd_en goes high and store the data in an 8 bit register.
12	Seminar: Students have to finalize the seminar at the start of the semester and should refer IEEE papers, Journal Papers etc.

Open Ended Problem

1. Representation of Filters using Different DSP Representation Systems
2. To calculate Iteration Bound, Loop Bound, Critical Path of any DSP system/Filter with/without algorithms.
3. Timing/Retiming Problems with/without algorithms.
4. Fold/Unfold the given architecture.

Major Equipments: Xlinx, HDL Designer,

List of Open Source Software/learning website:

www.nptel.com
www.nptel.ac.in

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website