GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (VLSI SYSTEM DESIGN) (42)
HDL BASED DESIGN WITH PROGRAMMABLE LOGIC
SUBJECT CODE: 2724204
SEMESTER: II

Type of course: Major Elective_III (VLSI Based Course)

Prerequisite:

- Background in digital logic design
- Prior knowledge of a programming language (e.g., "C" language) is a plus

Rationale: Useful to understand the Front End Design Flow.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2#	0	4	70	30	30	0	10	10	150

Content:

Sr. No.	Content	Total Hrs	% Weight
1.	**Introduction** Design Methodology, Level of Abstractions, Design Flow, Design Approaches, Design Styles, Design considerations, Design Qualities, EDA tools.	**5**	**10**
2.	**Introduction to HDL Based Design** Introduction, Definition, Digital System Implementation options and selection criteria, HDL based design flow.	**4**	**8**
3.	**VHDL** Introduction, VHDL Based Digital Design Flow, VHDL for Library, Entity, Architecture, Declaration, VHDL Concurrent and Sequential Syntax ,Language Elements, Different style of modellig, Designing Combinational Language Logic and Synchronous Logic.	**9**	**19**
4.	**Programmable Logic Devices** Full Custom Design, Semicustom Design, Programmable Logic Devices, Read Only Memory (ROM), Programmable Read Only Memory (PROM), and Programmable Logic Array (PLA), and Programmable Array Logic (PAL),CPLD Architecture & CPLDs available in Market, FPGA Architectures, New trends in FPGAs, Selection Criteria and comparative study of all available programmable logic.	**10**	**21**
5.	**State Machine Design** State Machine Modelling, Modelling a Moore FSM, Modelling a Mealy FSM	**5**	**10**
6.	**Simulation and Synthesis** Event-driven simulation, Cycle Based Simulator,Writing a test bench, A test bench example, Simulation modelling issues. What is synthesis, Synthesis in a Design Process RTL synthesis, Modelling for Synthesis versus Modelling	**9**	**19**

	for Simulation, Behavioral synthesis		
7.	**Verilog** Introduction, Different style of modeling.	**6**	**13**

Reference Books:

1 J. Bhasker, A VHDL Primer, PH/Pearson
2 J.Bhasker, A VHDL Synthesis Primer, Second Edition, Star Galaxy, 1998.
3 J.Bhasker, A Verilog HDL Primer, , Second Edition, Star Galaxy, 1999.
4 J.Bhasker, A Verilog Synthesis: A Practical Primer, Star Galaxy, 1998.
5 C. H. Roth, Digital System Design with VHDL, PWS/Brookscole
6 Stiphen M Trimberger, Field Programmable Gate Array Technology, Springer
7 Samir Palnitkar, Verilog HDL : A Guide to Digital Design and Synthesis, Pearson
8 J. Bhasker, A Verilog HDL Primer, BS Publication
9 Kevin Skahil, VHDL for Programmable Logic, Pearson
10 Wyane Wolf, FPGA Based System Design, Pearson
11 Douglass L Perry, VHDL : Programming By Example, Tata Mc Graw Hill
12 J. Armstrong and F.G.Gray, , VHDL design Representation and synthesis,Second Edition, PH/Pearson, 2000.

Course Outcome:

After learning the course the students should be able to:

- Use the Hardware Description Languages like VHDL and Verilog
- Implement the design from specification to netlist level
- Verify the design using simulators
- Understand the FPGA and CPLD architecture in depth
- Write the hardware descriptions in context of synthesis, device utilization and speed and power optimization
- Effectively Implement the design on FPGA
- Optimize the design using place and route concepts

Tutorial:

Perform and write down the tutorial related to VHDL.

Major Equipments: Xilinx ISE 14.2, FPGA Kit.

List of Open Source Software/learning website:

1 http:// www.actel.com/documents/nano_Technology_WP.pdf
2 http://nptel.ac.in/
3 http://testlab.ncue.edu.tw/tch/lecture/HDL
4 http://www.eecs.ucf.edu/
5 http://www.xilinx.com/
6 http://esd.cs.ucr.edu/labs/tutorial/
7 http://www.altera.com/education/training/courses
8 http://www.gmvhdl.com/VHDL.html

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website