GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (VLSI SYSTEM DESIGN) (42)
TESTING AND VERIFICATION OF VLSI DESIGN
SUBJECT CODE: 2724202
SEMESTER: II

Type of course : Testing and verification of VLSI chip.

Prerequisite **:** Basics knowledge of Digital Electronics and CMOS Design.

Rationale **:** Useful to understand the Testing and verification of VLSI Design.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2#	2	5	70	30	20	10	10	10	150

Content:

Sr. No.	Content	Total Hrs	% Weight
1.	**Introduction of Testing and Verification :** Testing Philosophy, Roll Of Testing, Digital And Analog VLSI Testing, VLSI Technology Trends Effecting Testing, Verification Importance, Reconvergence Model, The Human Factor, What Is Being Verified? Verification and Design Reuse, The Cost Of Verification. Testing Versus Verification.	8	18
2.	**Test Process and Equipment:** How To Test Chips? Types Of Testing, Automatic Test Equipment, Electrical Parametric Testing.	4	8
3.	**Test Economics and Product Quality:** Test Economics, Yield, Defect Level As A Quality Measure.	4	8
4.	**Fault Modeling:** Defects, Errors, And Faults, Functional Versus Structural Testing, Levels Of Fault Models, A Glossary Of Fault Models, Single Stuck-At Fault.	5	11
5.	**Fault Simulation :** Usage of fault simulators, Fault simulator in a VLSI design process, Fault simulation algorithms: Serial, Parallel, Deductive, Concurrent, Fault sampling	4	8
6.	**Combinational ATPG:** Structural vs. functional test, Definition of ATPG, Exhaustive algorithm, Random pattern generation, Boolean difference 3symbolic method, Path sensitization method, Computation complexity.	4	8
7.	**Design-for-Testability:** Definition, Ad-hoc DFT methods, Scan design, Scan flip-flop, Muxed-DFF, LSSD, Scan test vectors, Multiple scan registers, Hierarchical scan.	3	7
8.	**Verification Tools***:* Linting Tools, Simulators, Third-Party Models, Waveform Viewers, Code Coverage, Verification Languages, Revision Control, Issue Tracking, Metrics.	4	8
9.	**The Verification Plan:** The Role of the Verification Plan, Levels of Verification, Verification Strategies, From Specification to Features, From Features to Testcases, From Testcases to Test benches.	4	8

10.	**Delay Test:** Delay test problem, Path delay test, Transition Faults, Delay test methodologies, Test and diagnosis for Small-Delay Defects (SDDs).	2	4
11.	**IDDQ Current Testing :** History and motivation, Basic principle of IDDQ testing, Fault detected by IDDQ tests, Limitations of IDDQ testing	2	4
12.	**Memory Testing :** Motivation, Functional model of a memory, Fault models, March tests	2	4
13.	**Built-In Self-Test:** Motivation, BIST definitions, BIST process, BIST pattern generation, BIST response compaction, Aliasing definition	2	4

References:

1. M.L.Bushnell, V.D.Agrawal "Essentials of Electronic testing for Digital. Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers, New York, Boston, Dordrecht, London, Moscow, 2002.
2. Janick Bergeron, "Writing test benches functional verification of HDL models" Kluwer Academic Publishers, New York, Boston, Dordrecht, London, Moscow, 2002.
3. Jayaram Bhasker "A VHDL Primer" , P T R Prentice Hall Englewood Cliffs, New Jersey.

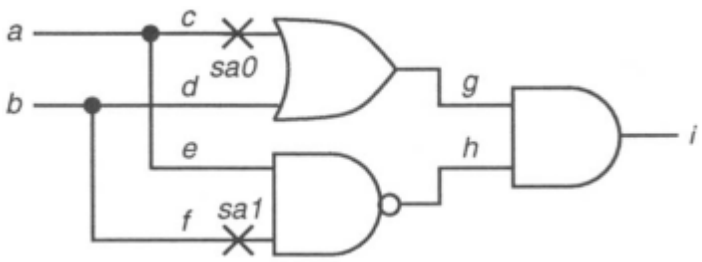
Course Outcome:

After learning the course the students should be able to:

1 Understand the basic concept of Testing and Verification.
2 Understand the importance of testing and verification.
3 Understand various types of Fault and its modeling.
4 Understand the various testing like IDDQ, Memory, and BITS etc.
5 Understand the concept of DFT.

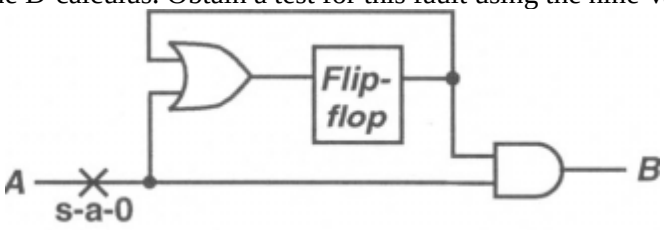
Open Ended Problem:

1. Imagine three-dimensional VLSI systems in the form of a cube, where the volume contains transistors and interconnects, and pins are placed on the surface. We assume that the problems of power dissipation and cooling have been worked out to make such a device possible. Derive Rent's rule for this device. Is the test problem for the cube more, or less, complex than that for the flat chip?
2. You are making microprocessor chips, and need to have a very low product failure rate in the field to control your warranty costs. Describe the various types of tests that you would use on the microprocessor chips at their various stages of processing.
3. Using test data analysis a chip production process has been characterized with fault density, f=1.45 faults/sq. cm, and fault clustering parameter, β=0.11 Given that the fault coverage of tests is 95%, calculate the defect level for a chip of 1 sq. cm area. What should the fault coverage be if the required defect level is: (a) 1,000 *ppm,* and (b) 500 *ppm.*
4. Show that the two faults *c* s-a-0 and *f* s-a-1 are equivalent in the circuit of following Figure.



5. Justify that verification is a necessary evil.
6. Justify that we can prove the present of fault bur not the absent of fault.
7. Significance of verification plan.
8. Prove that every singly-testable (i.e., nonrobustly testable) fault has a single-input change test.

9. Show that a test for the fault *A* s-a-0 in the circuit of following figure cannot be obtained using the five-valued logic of the D-calculus. Obtain a test for this fault using the nine-valued logic.



10. Prove that a fault that is untestable in the stand-alone combinational logic is also untestable in the sequential circuit.

List of Experiments:

1 Introduction to Testing & Verification Tolls.
2 Study of Concept of Verification Environment and its component by preparing an exhaustive test bench for all Basic Logic Gates.
3 Study of Concept of Verification Environment and its component by preparing an exhaustive test bench for Adder Circuit.
4 Study of Concept of Verification Environment and its component by preparing an exhaustive test bench for Multiplexer.
5 To verify sequential circuits like Flip-Flops with the testbench.
6 To verify sequential circuits like Counter with the testbench.
7 To verify sequential circuits like 3 to 8 Decoder with the testbench.
8 To prepare a complete test vector set for all stuck at faults in any one of the following systems:
  • Two bit adder
  • Two bit parity generator
  • 2:1 Multiplexer
9 To create an exhaustive test bench with generator, checker and golden reference model for Arithmetic Logic Unit(ALU)
10 Miniproject.

Major Equipments: Mentor Graphics, Tanner, Cadence, Synopsys, Xilinx Software

List of Open Source Software/learning website:

1 www.xilinx.com.
2 www.tannereda.com/t-spice-pro.
3 www.nptel.com.
4 www.mentor.com/india.
5 www.synopsys.com.
6 www.cadence.com/in

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website