GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (SIGNAL PROCESSING AND VLSI TECHNOLOGY) (26)

ALGORITHMS FOR VLSI PHYSICAL DESIGN AUTOMATION

SUBJECT CODE: 2722606

SEMESTER: II

Type of course: Physical Algorithm Based Course

Prerequisite: Basic knowledge of VLSI Chip Design and Graph Theory

Rationale: This course provides a platform for students to apply basic knowledge of algorithm to understand and implement complex physical design algorithms such as Circuit Partitioning, Floor planning, Placement, Grid and Global routing etc. This course gives insight into designing of various CAD Tools.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	0	2#	4	70	30	20	10	10	10	150

Content:

Sr No	Course Content	Teaching hours	Module weightage
1	**Introduction:** VLSI Design, The VLSI Design Process, Layout Styles, Difficulties in Physical Design, Definitions and Notation	4	9
2	**Circuit Partitioning:** Introduction, Problem Definition, Cost Function and Constraints, Approaches to Partitioning Problem, Other Approaches and Recent Work.	5	13
3	**Floor planning:** Introduction, Problem Definition, Approaches to Floor planning, Other Approaches and Recent Work.	5	13
4	**Placement:** Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Placement, Other Approaches and Recent Work.	5	13
5	**Grid Routing:** Introduction, Problem Definition, Cost Functions and Constraints, Maze Routing Algorithms, Line Search Algorithms, Other Issues, Other Approaches and Recent Work.	5	13
6	**Global Routing:** Introduction, Cost Functions and Constraints, Routing Regions, Sequential Global Routing, Integer Programming, Global Routing by Simulated Annealing, Hierarchical Global Routing, Other Approaches and Recent Work.	5	13
7	**Channel Routing:** Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Channel Routing, Other Approaches and	5	13

	Recent Work.		
8	**Layout Generation:** Introduction, Layout Generation, Standard-cell Generation, Optimization of Gate-matrix Layout, Programmable Logic Arrays, Other Approaches and Recent Work.	5	13
		39	100

Reference Books:

1. VLSI Physical Design Automation, Theory and Practice, Sadiq M. Sait and Habib Youssef. By world scientific press.
2. Algorithm for VLSI physical design automation by Sherwani and navneed- by Springer /B S Publication (2008).
3. N. Sherwani, Algorithms for VLSI Physical Automation, Third Edition, Kluwer, 1998.
4. S. H. Gerez, Algorithms for VLSI Design Automation, Wiley, 1998.
5. A. Micozo, Digital Logic Testing and Simulation, Second edition, Wiley, 2003.
6. S. M. Sait and H. Yousuf, Iterative Computer Algorithm with Applications in Engineering, Wiley/IEEE, 2002.
7. C. Visweswariah and S. Duvall, Computer Aided Optimization of Digital Integrated Circuits, Wiley, 2002.
8. G. De Micheli, Synthesis and Optimization of Digital Circuits, Mcgraw-Hill International, 1994.

Course Outcome:

After learning the course the students should be able to:

1 Understand the concept of different constraint, cost functions and optimization.
2 Optimization of VLSI Design in using Circuit Partitioning, Floor planning and placement.
3 Use of different algorithm in design of CAD tools for VLSI Design.
4 Different styles of routing for optimization of Area.
5 Understand various CAD Tools.
6 Suggest Modification in any of the algorithm.

List of Experiments and Open Ended Problems:

Perform experiments in either Scilab or Matlab.

1 Introduction to Various CAD Design Tools and its comparisons.
2 Implementation of Dijkstra's routing algorithm.
3 Implementation of the Kernighan Lin Algorithm for circuit partitioning.
4 Implementation of the Fiduccia Mattheyses Algorithm for circuit partitioning.
5 Implementation of the Simulated Annealing Algorithm.
6 Implementation of the Genetic Algorithm.
7 Implementation of Yoshimura and Kuh algorithm.
8 Implementation of the Linear Ordering Cluster Growth Algorithm.
9 Implementation of the Unconstrained Algorithm for channel routing.
10 Implementation of the vertical constrained Algorithm for channel routing.
11 Seminar report for a given research topic.
12 Case study: Modification in any existing algorithm.

Major Equipments/software: SciLAB / MATLAB

List of Open Source Software/learning website:

1. http://wwwhome.ewi.utwente.nl/~gerezsh/cadvlsi/book.html
2. http://www.personal.kent.edu/~rmuhamma/GraphTheory/graphTheory.htm
3. http://compprog.wordpress.com/2007/11/09/minimal-spanning-trees-prims-algorithm/
4. http://www.people.vcu.edu/~gasmerom/MAT131/mst.html
5. http://www.personal.kent.edu/~rmuhamma/GraphTheory/MyGraphTheory/trees.htm
6. http://graphics.stanford.edu/courses/cs448b-02-winter/lectures/treesgraphs/tree.graph.pdf
7. http://www.slideshare.net/purpleinkredshirt/introduction-to-graph-theory
8. http://lecturesppt.blogspot.in/2011/09/graphs-and-algorithms-pdf-ppt-slides.html
9. http://www.authorstream.com/Presentation/ankush85-159135-nphard-nphard171-175-education-ppt-powerpoint/
10. http://www.authorstream.com/Presentation/nitinmishra10-83453-complexity-algorithm-data-structure-algorithms-lecture-3-education-ppt-powerpoint/

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website