GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (SIGNAL PROCESSING AND VLSI TECHNOLOGY) (26)/ ELECTRONICS & COMMUNICATION (VLSI SYSTEM DESIGN) (42)

CMOS CIRCUIT DESIGN – II

SUBJECT CODE: 2722602

SEMESTER: II

Type of course: Advanced MOSFET based analog circuit design

Prerequisite: MOSFET modeling and basic CMOS circuit design

Rationale: This course provides a platform for students to apply basic knowledge of working of MOSFETs to analyze and design complex analog and mixed signal circuits such as phased locked loops, bandgap references, analog to digital converters and digital to analog converters, memory circuits, switched capacitor circuits, comparator circuits and low noise amplifiers, etc.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2#	2	5	70	30	20	10	10	10	150

Content:

Sr No	Course Content	Teaching hours	Module weightage
1	**Bandgap References:** General Considerations, Supply-Independent Biasing, Temperature-Independent References, PTAT Current Generation, Constant Gm Biasing, Speed and Noise Issues, Case Study	**06**	**12%**
2	**Memory Circuits:** Introduction, Sensing Basics, Folded Array, Chip Organization, Sense Amplifier Design, Row/Column Decoder, Row Drivers, SRAM Cell, ROM, Floating Gate Memory, Sensing using Modulation: Examples of DSM, Using DSM for sensing in Flash Memory, Sensing Resistive Memory, Sensing in CMOS Images	**08**	**15%**
3	**Phase-Locked Loops:** Simple PLL, Charge-Pump PLLs, Nonideal Effects in PLLs, Delay-Locked Loops, Applications	**08**	**15%**
4	**Digital-Analog and Analog-Digital Converters:** Introduction and Characterization of DAC, Parallel DAC, Introduction and Characterization of ADC, Serial ADC	**06**	**12%**
5	**Introduction to Switched-Capacitor Circuits:** General Considerations, Sampling switches, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor	**08**	**15%**

	Common-Mode Feedback		
6	**Low noise Amplifiers:** General considerations, problem of input matching, LNA topologies, Gain switching, Band switching, High-IP2 LNAs, Nonlinearity calculations.	**12**	**24%**
7	**Nonlinear Analog Circuits:** Basic CMOS Comparator Design, Characterizing the Comparator, Clocked Comparators, Adaptive Biasing, Analog Multipliers	**04**	**7%**

Reference Books:

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH
2. CMOS Circuit Design, Layout, and Simulation, R. Jacob Baker, Wiley, 2nd Edition
3. RF Microelectronics, Behzad Razavi,Pearson,2nd Edition

Course Outcome:

1 To analyze and design bandgap reference circuit.
2 To analyze and design various blocks of memories.
3 To analyze and design SRAM.
4 To analyze and design DRAM.
5 To study operation of basic and charge pump PLL as well as related design issues.
6 To study operation of switched capacitor circuits as well as related design issues.
7 To study operation of LNA as well as related design issues.
8 To study operation of CMOS comparator circuits as well as related design issues.

List of Experiments:

Perform experiments 1 to 11 in 180 nm technology.

1 To simulate self-biased supply independent band-gap reference circuit with and without startup circuit, and obtain its current response as a function of variation in supply voltage.
2 To verify through simulation that NMOS is poor conductor of '1', PMOS is poor conductor of '0,' and transmission gate is good conductor of '1' and '0'.
3 To obtain ON resistance of following devices when used a switch using simulation:
   1. NMOS
   2. PMOS
   3. Transmission Gate
4 To obtain the error in sampled voltage when following devices used a switch using simulation:
   1. NMOS
   2. PMOS
   3. Transmission Gate
5 To study and simulate dummy device based charge injection cancellation technique. Obtain the error in sampled voltage.
6 To simulate switched capacitor amplifier circuit.
7 To simulate basic clock signal based sense amplifier circuit and measure its performance parameters.
8 To simulate and analyze charge pump PLL.
9 To simulate regenerative feedback based CMOS comparator circuit and measure its performance parameters.

10 To simulate 1-bit DRAM and measure its performance parameters.
11 To simulate 1-bit SRAM and measure its performance parameters.
12 Perform above experiments in 90 nm technology also and compare as well give comments on your results.
13 Seminar report for a given research topic.

Open Ended Problems:

1 Design a switched capacitor based integrator.
2 Design a phase detector using D Flip-flop for PLL.
3 Design a basic charge pump PLL.
4 Design a simpledelay locked loop.
5 Design a reactance cancelling LNA.
6 Design a multiply by two circuit.
7 Design an 8 bit Flash ADC.
8 Design self-biased supply independent band-gap reference circuit with startup circuit.
9 Design a Cascode CS LNA.
10 Design a 3 bit current steering DAC.
11 Design a 4 bit charge scaling DAC using split array.
12 Design a clocked comparator based on basic latch.
13 Design a preamp and decision circuit for comparator.
14 Design a self biasing differential amplifier used as the comparator output buffer.

Major Equipments: C.R.O., Function Generator, Power Supply, Multimeter, Digital Storage Oscilloscope

List of Open Source Software/ Learning website:
1. ngspice/multisim (software)
2. www.nptel.ac.in
3. www.ocw.mit.edu
4. www.mosis.com
5. www.berkeley.edu

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website