GUJARAT TECHNOLOGICAL UNIVERSITY

INSTRUMENTATION AND CONTROL (APPLIED INSTRUMENTATION) (03)
ADVANCE VLSI DESIGN
SUBJECT CODE: 2720314
SEMESTER: II

Type of course: Major Elective II

Prerequisite: Digital Logic Design

Rationale: This course introduces overview and fundamentals of VLSI design and provides the essential knowledge about the main themes so the students will be able to readily apply this knowledge in industry or research.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	PA (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2#	2	5	70	30	20	10	10	10	150

Content:

Sr. No.	Topics	Teaching Hrs.	Module Weightage
1	**Introduction to VLSI Design and Verilog:** Conventional approach to digital design, VLSI design, ASIC design flow, Role of HDL, Verilog as an HDL, Levels of design description, Concurrency, Simulation and synthesis, Functional verification, System tasks, Programming language interface, module, Simulation and synthesis tools, Test benches.	03	0-5%
2	**Language Constructs and Conventions in Verilog:** Keywords, Identifiers, White space characters, Comments, Numbers, Strings, Logic values, Strengths, Data types, Scalars and vectors, Parameters, Memory, Operators, System tasks.	03	0-5%
3	**Architecture of FPGA:** Generic FPGA architecture, Architectural overview, Configuration, I/O capabilities, Program design flow, Device programming, Design implementation using FPGA, Simulation, Compilation, Floor planning and architecture design: floor planning methods, off-chip connections, High –level synthesis, Architecture testing.	04	5-10%
4	**Gate Level Modelling:** Basic gate primitives, Module structure, Tri state gates, Array of instances of primitives, Design of flip-flops with gate primitives, Delays, Strengths and contention resolution, Net types, Design of basic circuits.	05	10-20%
5	**Modelling at Data Flow Level:** Continuous assignment structures, Delays and continuous assignments, Assignment to vectors, Operators.	06	10-20%
6	**Behavioural Modelling :** Operations and assignments, Functional Bifurcation, Initial, always and wait constructs, Assignments with delays, Multiple always blocks, Design at behaviour level, Blocking	07	10-20%

	and non-blocking assignments, Case statement, Simulation flow, If and if-else, assign-de assign, repeat, disable and force-release constructs, For, while and forever loops, Parallel blocks, Event.		
7	**User Defined Primitives and FSM:** User-defined primitives (UDP), Mealy and Moore finite state machine.	05	5-20%
8	**Architecting Speed, Area and Power:** High throughput, Low latency, Timings, Rolling Up the pipeline, Resource sharing, Impact of reset on area, Clock control, Input control, Reducing the voltage supply, Dual edge triggered flip-flops.	08	10-25%
9	**Clock Domains:** Crossing clock domains, Gated clocks in ASIC prototypes.	03	0-5%

Reference Books:

1. Design through Verilog HDL, Wiley student edition, T. R. Padmanabhan and B. Bala Tripura Sundari
2. Steven Kilts, Advanced FPGA Design, John Wiley & Sons, 2007
3. Clive Max Filed, The Design.Warriors Guide to FPGA, Elsevier, 2004
4. Verilog HDL by Samir Palniker.
5. Digital Design &Implementation with Field Programmable Devices by Zainalabedin Navabi.
6. Design recipes for FPGAs by Dr. Peter R. Wilson, Elsevier.

Course Outcome:

After learning the course the students should be able to

1. Understand the main elements of hierarchical VLSI design namely integrated circuit technology, approaches to system design, architectural issues, design implementation and layout.

2. Ability to apply VLSI design methodology for the design of application specific integrated circuits.

3. The ability to analyse the effect of future integrated circuit technologies on device parameters.

List of Experiments:

Simulation and synthesis of various combinational and sequential circuits in verilog HDL using Xilinx tool.

Open Ended Problem: Solution of the open ended problem(s) in guidance of course instructor is mandatory. Few of the problems are specified as under.

1. Implementation of PID controller in FPGA.
2. Design and optimization of arithmetic logic unit (ALU) for area, speed and power in FPGA.
3. Implementation of real time embedded system on FPGA.
4. Implementation of digital filters, transforms and algorithms in FPGA.
5. Implementation of simple processor and soft core on FPGA.
6. Implementation of a PS/2 keyboard reader on the FPGA and one other simple (open ended) design on the FPGA.
7. Implementation of a video capture and display system using the FPGA board, a camera and a VGA monitor.
8. Implementation of a SoC in a hardware software co- design fashion.

Major Equipment:

Computer Laboratory, FPGA board

List of Open Source Software/learning website:8

- Xilinx
- Altera
- NTPEL

Review Presentation(RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.