GUJARAT TECHNOLOGICAL UNIVERSITY

BIO MEDICAL ENGINEERING (31)

DIGITAL SYSTEM DESIGN

SUBJECT CODE: 2713111

SEMESTER: I

Type of course: Major Elective

Prerequisite: Digital electronics

Rationale: The course deals with how digital systems can be built using available hardware and software tools. Fundamentals, architecture and programming of FPGA and CPLD is covered. It also explains concept of ASIC and SoC

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	PA (V)		PA (I)		
						ESE	OEP	PA	RP	
3	2	2	5	70	30	20	10	20	0	150

Content:

Sr. No.	Topics	Teaching Hrs.	Module Weightage
1	Design of combinational circuit building blocks: synthesis of logic functions using multiplexers, demultiplexers, binary encoders code converters, arithmetic comparison circuits, Shift registers, Timing ,Asynchronous counters and synchronous counters, state diagram, design of finite state machines, serial adder, Asynchronous sequential circuits, analysis and synthesis, state diagram	6	15%
2	Basic concepts of hardware description languages, Hierarchy, Concurrency, logic and delay modelling, Structural, Data-flow and Behavioral styles of hardware description, Architecture of event driven simulators, Syntax and Semantics of VHDL/verilog, Variable and signal types, arrays and attributes, Operators, expressions and signal assignments, Modules, nets and registers, Tasks and functions, Examples of design using VHDL/Verilog	10	25%
3	Programmable Logic: Introduction, programmable logic devices (PLDs), SPLDs, CPLDs, fundamentals of PLD circuits, PLD architectures: Progrmmable Read Only Memories (PROMs), Programmable Array Logic (PAL), ALTERA CPLDs	8	20%
4	Field Programmable Gate Arrays, Introduction to FPGA, Logic Block Architecture, Routing Architecture, Programmable Interconnections, Design Flow, Xilinx Spartan architecture, Xilinx Virtex Architecture, Altera, Programming FPGA's.	10	25%
5	ASIC Design, Custom IC Design Flow, logical and physical design steps, standard cells, ASIC Cell libraries, Gate Array Designs, Programming Technologies, Introduction to IP cores.	6	15%

Reference Books:

1. Park K. Chan / Samiha Mourad, "Digital Design using Field Programmable Gate Arrays", Pearson, 1994 (Unit-I)
2. Ronald J Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems: Principles & Applications", 10th Edition, Pearson, 2009 (Unit-II)
3. Stephen Brown Zvonko Vranesic – Fundamentals of Digital Logic with VHDL design, McGraw Hill – 2000 (Unit I & II).
4. Stephen D. Brown, Robert J Francis, Jonathan Rose, Ivonko G. Vranesic, "Field Programmable Gate Arrays", Springer International Edition, First Indian Print 2007(Unit III & IV)
5. Wayne Wolf, "FPGA-based System Design", Pearson Education, First Impression, 2009 (Unit V)
6. Stephen M. Trimberger, "Field Programmable Gate Array Technology" Springer International Edition", First Indian Reprint 2007.
7. Michel John Sebastian Smith "Application – Specific Integrated Circuits", Pearson Education, First Indian reprint 2000.
8. Ian Grout, Digital Systems Design with FPGAs and CPLDs, Elsevier
9. Samir Palnitkar, "Verilog HDL - A Guide to Digital Design and Synthesis"
10. M.J.S .Smith, - " Application - Specific Integrated Circuits " - Addison –Wesley Longman Inc., 1997

Course Outcome:

After learning the course the students should be able to:

1. The student will use theory of combinational circuits for writing VHDL program.
2. The student will exhibit the knowledge of sequential circuits for building a self-test.
3. The student will show the skills of designing analog and digital VLSI ICs.

List of Experiments:

1. Take any combinational circuit and write VHDL/Verilog code for it.
2. Design a clock debouncing circuit and implement it.
3. Design a system to implement a self-test for any sequential circuit.
4. Interface a 4×4 matrix keypad with the CPLD and display the pressed key on the Liquid Crystal display interfaced with the same CPLD.
5. To implement decade counter on any FPGA experimental Kit and verify the output on seven segment LED display.
6. Implement matrix multiplication using FPGA.

Open Ended Problems :

1. Design a FPGA-Based Medical Image Registration
2. Design a FPGA-based 8-channel arbitrary waveform generator for medical ultrasound research activities
3. Design a FPGA based real-time image segmentation for medical systems and data processing
4. Design a FPGA based data acquisition system for medical imaging
5. Design a FPGA based data acquisition system for Bio signals
6. Design a 8 Point Fast Fourier Transform Algorithm using FPGA with Verilog/VHDL
7. Develop an algorithm for any biomedical application using Verilog or VHDL.

etc.

Major Equipment: Xilinx Virtex kit